Embedded Ferroelectric Memory Using a 130-nm 5 Metal Layer Cu / FSG Logic Process

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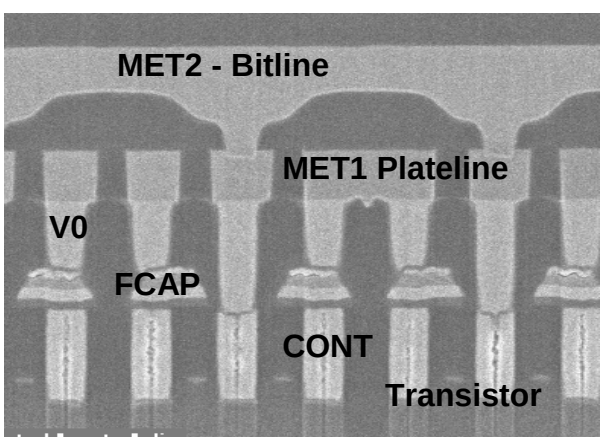
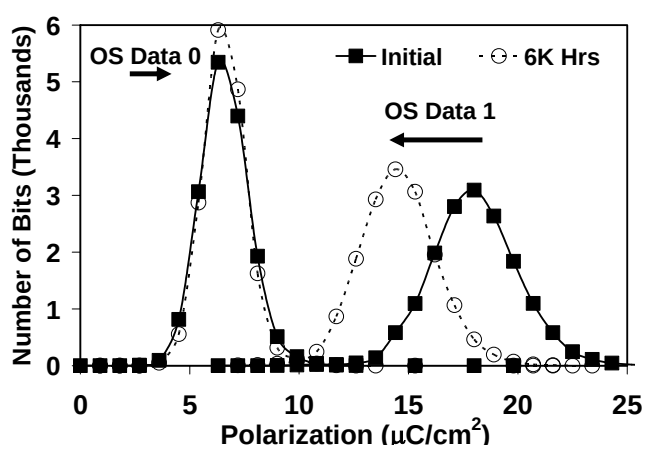
Unlike conventional embedded memory options (eFlash, eDRAM, or SRAM), embedded ferroelectric memory (eFRAM) offers the combination of fast-write times (<35ns) and low-power, non-volatile data retention. These features, in combination with eFRAM's proven reliability, benefit the portable-electronics consumer through increased battery life and instant-on functionality. Further, eFRAM functionality is cost effective because the cell size is significantly (~3x) smaller than an SRAM cell and the ferroelectric memory module is implemented with only a 2 mask adder to standard CMOS. In this paper we will describe functional eFRAM memories created using a 130nm, 5 metal level, Cu / FSG process flow.

The FRAM module, which consists of a ferroelectric capacitor (FCAP) and through via (VIA0), is inserted between the contact and first metal layers of a standard logic process flow. The capacitor stack is composed of a TiAlN diffusion barrier, Ir bottom electrode, MOCVD $Pb(Zr,Ti)O_3$ (PZT) ferroelectric, IrOx/Ir top electrode and TiAlN hardmask. The capacitor area is defined using the FECAP mask and etched using a multi-step reactive-ion etch process. Following capacitor isolation, an AlOx diffusion barrier, SiN etch stop layer, and SiO_2 interlayer dielectric are deposited followed by chemical-mechanical planarization. The second mask, VIA0, is used to define multi-level W vias which create electrical connection from the first metal level to either the ferroelectric capacitor or the underlying contact. For embedded FRAM products, there are no modifications to the standard front-end or back-end processes. As a result of the integration sequence and low-thermal budget of the ferroelectric module, the CMOS electrical properties are not impacted by the addition of the FRAM module and the standard design libraries can be used for eFRAM products.

The electrical properties of the ferroelectric are maintained even after 5-level metal Cu backend process and the properties of the capacitors are area independent down to small areas ($0.2\mu m^2$). In addition, the bit distribution properties of capacitors were measured using a special test circuit. These properties were studied after stressing (endurance and imprint) and the results are promising.



Cross sectional SEM showing the FRAM module integrated between CONT and MET1.



Memory array distribution measurement of the opposite-state Data 0 and Data 1 as a function of time at 125°C bake. Data 0 is stable, but Data 1 degrades over time.