A Fully CMOS Integrated Ionic Mass Transport Memory

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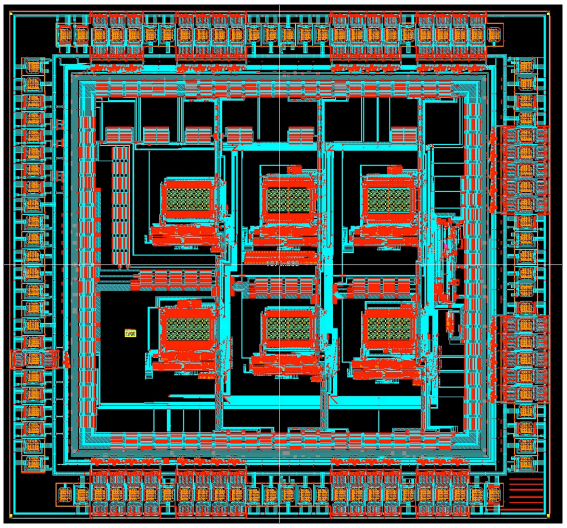
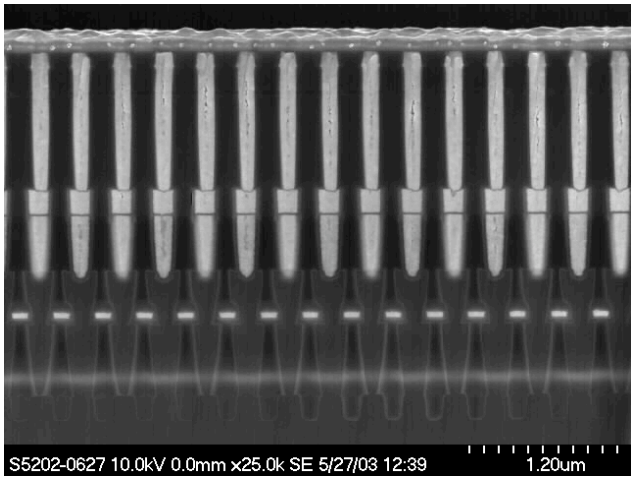
The Ionic Mass Transport Cell (IMTC) is a resistance variable device that can be used as a memory storage element. This is a new technology that relies on a resistance change which is mediated by transport of metal ions into and out of a superionic conducting channel. We describe the characterization of an IMTC based memory fully integrated into a CMOS chip. The test chip consists of six 256K arrays using 0.15um design rules, an $8F^2$ array architecture, single polycide, double metal, twin well CMOS with a 6 nm gate oxide access device. The process is such that the active memory element is built after the second metal level and all significant thermal processing. The yield of functional bits in an array is in excess of 99%. The typical failures are random single bits that fail to erase. Individual bits have been cycled greater than 10^{10} times, are nonvolatile and operate at DRAM speeds.



IMTC test chip.



IMTC array cross section.